REMARKS

Reconsideration of this application, based on this amendment and these following remarks, is respectfully requested.

Claims 1, 3 through 8, 10, 15, 16, 19 through 22, and 43 through 48 are now in this case. Claims 1, 3 through 5, 8, 10, 15, 16, 19, 21, and 22 are amended. Claims 2, 9, 11 through 14, 17, 18, and 23 through 42 are canceled. Claims 43 through 48 are added.

Claims 1 through 6, 8 through 13, 15 through 20, 22 through 26, 28 through 34, and 36 through 42 were rejected under §102 as anticipated by the Bruce et al. reference[1]. Claims 7, 14, 21, 27, and 35 were rejected under §103 as unpatentable over the Bruce et al. reference in view of the Kramer reference[2]

Claim 1 is amended to overcome the rejection. Amended claim 1 now recites the non-volatile memory as having a plurality of erase units, each including a plurality of programming units arranged in a sequence;[3] similarly, a first logical unit includes a plurality of logical sub-units arranged in a sequence.[4] Amended claim 1 now also includes the step of grouping the programming units into a plurality of groups of programming units,[5] and the additional step of, after the writing of the contents of first and second logical sub-units into programming units of a first group of programming units, writing the contents of a third logical sub-unit into a second programming unit of a second group of programming units, with the third logical sub-unit being earlier in the sequence of logical sub-units than the second logical sub-units.[6] No new matter is presented by this amendment, considering the clear support for the added limitations, as noted.

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[1] U.S. Patent No. 6,000,006, issued December 7, 1999 to Bruce et al.

[2] U.S. Patent No. 6,182,239 B1, issued January 30, 2001 to Kramer.

[3] *See* specification of S.N. 10/679,008, *as published as* U.S. Patent Application Publication US 2004/0103241, paragraph [0040]. All references to the specification in this paper will be made relative to this U.S. Patent Application Publication.

[4] *See* specification, *supra,* paragraphs [0051] through [0053].

[5] *See* specification, *supra,* paragraphs [0044] through [0050].

[6] *See* specification, *supra,* paragraphs [0046], [0055].

The method of claim 1 enables substantial advantages over conventional flash memory operation.[7] Specifically, this inventive method efficiently permits out-of-sequence write operations within a given physical block (erase unit), even in a flash memory of a type (*e.g.,* NAND memory) in which out-of-sequence write operations are prohibited.[8]

Claim 2 is canceled, and claims 3 through 5 are amended, for consistency with the amendment to claim 1. Claim 8 is amended to now depend on amended claim 1, and for consistency with amended claim 1; claims 9 and 11 through 14 are canceled accordingly, and claim 10 is amended to depend on amended claim 1 directly and for consistency with that claim.

Applicants submit that amended claim 1 is novel and patentably distinct over the Bruce et al. and Kramer references, on the grounds that the combined teachings of these references fall short of the requirements of amended claim 1.

Specifically, Applicants submit that the Bruce et al. reference nowhere discloses the grouping of programming units within an erase unit into a plurality of groups of programming units, as required by amended claim 1. Rather, the Bruce et al. reference discusses only pages (*i.e.,* programming units) and blocks (*i.e.,* erase units), for example by comparing page re-mapping to block re-mapping.[9] Nowhere does the Bruce et al. reference anywhere mention the arrangement of its pages into groups within a physical block. Accordingly, the Bruce et al. reference cannot possible disclose the step of writing the contents of a third logical sub-unit into a programming unit in a second group of programming units of the first erase unit, this third logical sub-unit being earlier in a sequence of logical sub-units than a second logical sub-unit whose contents are previously written into a first group of programming units in that first erase unit, as required by amended claim 1. Accordingly, Applicants submit that amended claim 1 is novel over the Bruce et al. reference.

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[7] *E.g.,* specification, *supra,* paragraphs [0008] through [0011].

[8] Specification, *supra,* paragraphs [0050].

[9] Bruce et al., *supra,* column 1, line 41 through column 2, line 31; column 9, line 57 through column 10, line 45 (*e.g.,* "FIG. 8 shows that block-granularity rather than page-granularity for re-mapping and wear-leveling provides additional bits for an error-correction code.")

Nor does the Kramer reference anywhere disclose such grouping of programming units within an erase unit, as required by amended claim 1. The Kramer reference was cited as teaching MLC NAND flash memories,[10] but nowhere provides any teachings regarding the elements of amended claim 1 that are not taught by the Bruce et al. reference, as discussed above. Accordingly, Applicants submit that even if the teachings of the Kramer reference are combined with those of the Bruce et al. reference, these combined teachings would fall far short of the requirements of amended claim 1 and its dependent claims.

Applicants further respectfully submit that there is no suggestion from these references, or elsewhere in the prior art, to modify the teachings of these references in such a manner as to reach amended claim 1 and its dependent claims. This lack of suggestion is apparent from the Bruce et al. reference especially, in that the reference makes no mention of the problems that arise in flash memories that prohibit out-of-sequence write operations, and as such cannot possibly suggest the solution for efficiently dealing with writes of updated data in such memories, as provided by the method of amended claim 1 and its dependent claims.

For these reasons, Applicant submit that amended claim 1 and its dependent claims 3 through 8, and 10, are not only novel but are patentably distinct over the references of record in this case.

New claims 43 through 45 depend on amended claim 1, and are added to more completely cover all aspects of Applicants' invention. New claim 43 further recites, relative to amended claim 1 upon which it depends, additional method steps related to the determining of whether an additional group of programming units is available if necessary, and if not, the merging of the contents of the previously written contents into a second erase unit.[11] Claim 44 further specifies the nature of the merging step, relative to claim 43 upon which it depends.[12] Claim 45 further recites the additional steps of determining whether additional updates are to be written, and the repeating of the steps of claim 43 or additional merging of the contents.[13] Considering the clear support for these claims in the specification, Applicants submit that no new matter is added. Applicants further submit that these new claims 43 through 46 are further novel and patentably distinct over the prior art of record, as neither of the applied references disclose or suggest their additional limitations.

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[10] Office Action of January 18, 2006, page 8.

[11] *See, e.g.,* specification, *supra,* paragraphs [0070] and [0071].

[12] *Id.*

Independent apparatus claim 22 is also amended to overcome the rejection, and to more completely cover Applicants' invention. Amended claim 22 now recites that the non-volatile memory includes a plurality of erase units that each include a plurality of programming units, in combination with means for controlling the writing of contents into the memory according to groups of programming units within each erase unit.[14] The claim also requires that the controlling means effect such controlling by way of a sequence of operations including, *inter alia,* the writing of contents of a third logical sub-unit into a second group of programming units of a first erase unit, the first erase unit also having a first group of programming units into which contents were previously written. Applicants submit, because of the clear support in the specification for the controlling means and also for the operations performed by this controlling means, as discussed above relative to amended claim 1, that no new matter is presented by this amendment to claim 22.

The system of amended claim 22 provides similar advantages, over conventional flash memory devices, as those discussed above relative to amended claim 1. More specifically, the system of claim 22 greatly improves the efficiency with which the contents of a flash memory may be updated over time, even in flash memory devices in which out-of-sequence programming is not permitted. This improvement in efficiency stems directly from the use of groups of programming units within a single erase unit, as recited in amended claim 22.

Claim 15 is amended to now depend on amended claim 22, and to recite that the controlling means comprises code devices for performing the sequence of operations, and a processor for accessing and executing those code devices.[15] Claims 16 and 19 are amended to depend on amended claim 22, and for consistency with that claim. No new matter is presented by these amended claims 15, 16, and 19, considering the clear support for their limitations in the specification.

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[13] *See, e.g.,* specification, *supra,* paragraph [0069].

[14] An example of the controlling means is described in the specification, *supra,* paragraph [0075].

For similar reasons as discussed above relative to amended claim 1, Applicants submit that amended claim 22 and its dependent claims are novel and patentably distinct over the Bruce et al. and Kramer references.

Applicants submit that the Bruce et al. reference nowhere discloses the grouping of programming units within an erase unit into a plurality of groups of programming units, much less any means for controlling the writing of contents into the memory according to such groups, as required by amended claim 22. The teachings of the Bruce et al. reference relative to the organization of its flash memory is limited to the organization and mapping of pages (*i.e.,* programming units) and of blocks (*i.e.,* erase units).[16] The Bruce et al. reference therefore necessarily fails to disclose the controlling of the writing of contents into a memory, much less involving the operation of the writing of contents of a third logical sub-unit into a programming unit in a second group of programming units of the first erase unit, this third logical sub-unit being earlier in a sequence of logical sub-units than a second logical sub-unit whose contents are previously written into a first group of programming units in that first erase unit. Accordingly, Applicants submit that amended claim 22 is novel over the Bruce et al. reference.

As previously discussed, the Kramer reference fails to add any teachings to those of the Bruce et al. reference in this regard. Applicants therefore submit that the combined teachings of the Bruce et al. and Kramer references fall far short of the requirements of amended claim 22 and its dependent claims.

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[15] *See e.g.,* specification, *supra,* paragraph [0072].

[16] Bruce et al., *supra,* column 1, line 41 through column 2, line 31; column 9, line 57 through column 10, line 45 (*e.g.,* "FIG. 8 shows that block-granularity rather than page-granularity for re-mapping and wear-leveling provides additional bits for an error-correction code.")

Applicants further respectfully submit that there is no suggestion from these references, or elsewhere in the prior art, to modify these combined teachings in such a manner as to reach amended claim 1 and its dependent claims. No mention is made, in either reference, of any limitations in flash memories that prohibit out-of-sequence programming, and therefore there is no suggestion to group pages within blocks, to use the vocabulary of the Bruce et al. reference. For these reasons, Applicant submit that amended claim 22 and its dependent claims 15, 16, and 19 through 21, are novel and patentably distinct over the references of record in this case.

New claims 46 through 48 are added in this Amendment to depend on amended claim 22, to more completely cover all aspects of Applicants' invention. The limitations of new claims 46 through 48, relative to claim 22 upon which they depend, correspond substantially to those of new claims 43 through 46 discussed above. For similar reasons, Applicants submit that these new claims 45 through 48 are also supported by the specification and therefore present no new matter, and also that these new claims are further novel and patentably distinct over the prior art of record in this case.

Claims 23 through 42 are canceled, without prejudice to their presentation in a continuing application, to advance the prosecution of this application.

The prior art cited as pertinent but not applied has been considered, but is not felt to come within the scope of the claims now in this case.

For these reasons, Applicants respectfully submit that the claims now in this case are in condition for allowance. Reconsideration of this application is therefore respectfully requested.

Respectfully submitted,

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May 18, 2006

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